Sequential Circuit: Flip Flops

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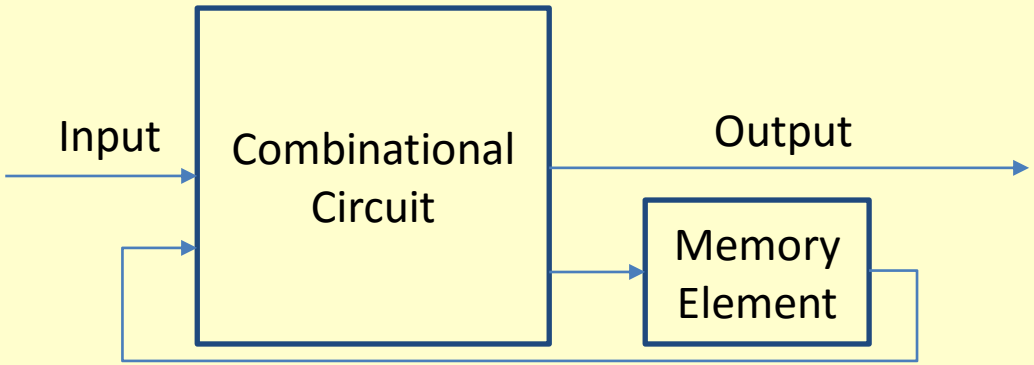
Sequential Circuit

A Sequential circuit is a combinational circuit with memory or storage element in feedback

i.e Sequential circuit' output depends on inputs as well as previous state of storage element.

Synchronous Sequential Circuit: Behaviour of the system depends on inputs (external and internal state) only at discrete instants of time. Storage elements used are clocked Flip Flops

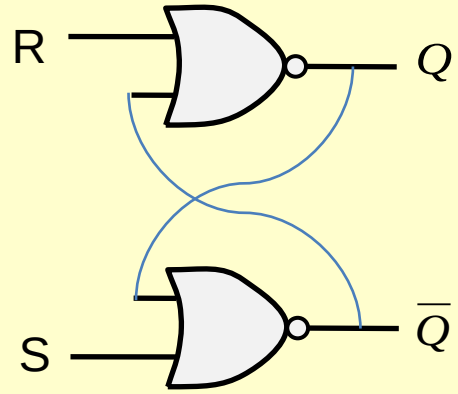
Asynchronous Sequential Circuit: Behaviour of the system depends on inputs (external and internal state) at any time. Storage element used are time delay elements and latches



Sequential Circuit

Latch

- Latch holds 1 bit of information
- Two outputs are complementary
- Inputs are S and R which Sets (output 1) and Resets (output 0) the latch
- S=R=1 is invalid in which rule of complementary output breaks



SR Latch using NOR gate

Characteristics table of SR Latch

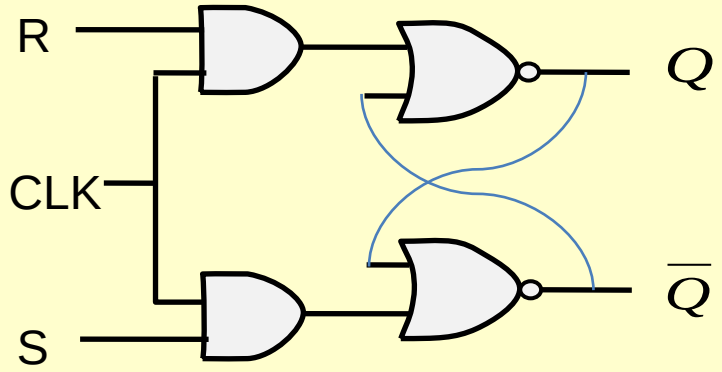
S	R	Q_{n+1}	
0	0	Q_n	No Change
0	1	0	Reset
1	0	1	Set
1	1	Invalid	

Full State table of SR Latch

S	R	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	invalid
1	1	1	invalid

SR Flip Flop

- In Latch, spurious inputs can cause output change at time.
- A clock pulse (in AND to inputs) ensures that inputs are applied only when clock pulse is present



SR FF

Characteristics table of SR FF

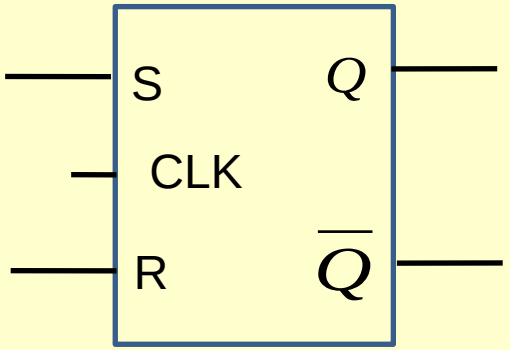
S	R	Q_{n+1}	
0	0	Q_n	No Change
0	1	0	Reset
1	0	1	Set
1	1	Invalid	

Full State table of SR FF

S	R	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	invalid
1	1	1	invalid

$$Q_{n+1}(J,K,Q_n) = \sum(1,4,5) + \phi(6,7)$$

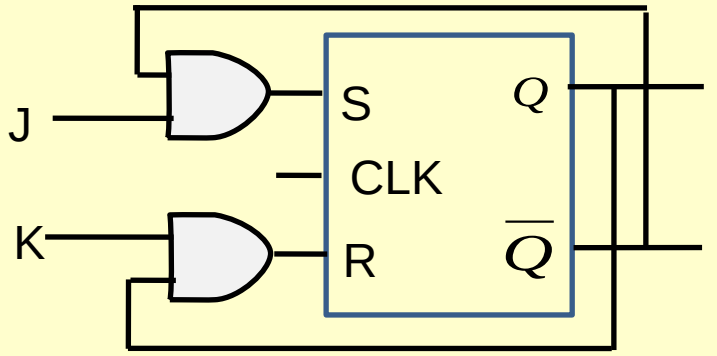
SR Characteristics equation $Q_{n+1} = S\overline{Q} + \overline{R}Q_n;\ \text{and}\ SR \neq 1$



SR Flip Flop symbol

JK Flip Flop

- JK is modification of SR FF for invalid input combination
- For J=K=1, output Toggles (complements)



Characteristics table of JK FF

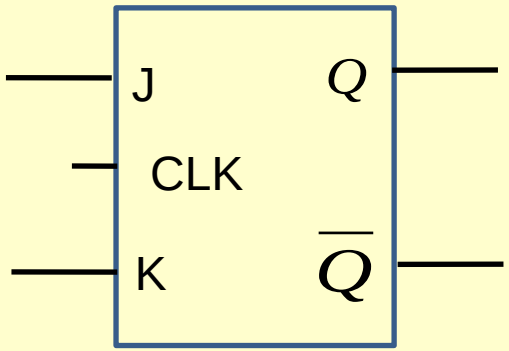
J	K	Q_{n+1}	
0	0	Q_n	No Change
0	1	0	Reset
1	0	1	Set
1	1	$\overline{Q_n}$	Toggle

Full State table of JK FF

J	K	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

$$Q_{n+1}(J,K,Q_n) = \sum(1,4,5,6)$$

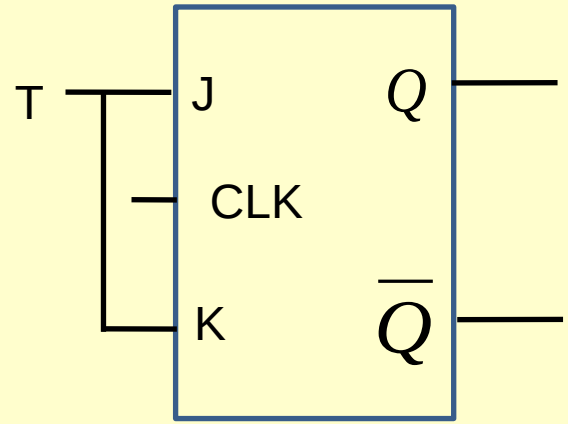
JK Characteristics equation $Q_{n+1} = J\overline{Q_n} + \overline{K}Q_n$



JK Flip Flop symbol

T Flip Flop

- T FF is JK FF with J=K
- For T=1, output Toggles (complements)



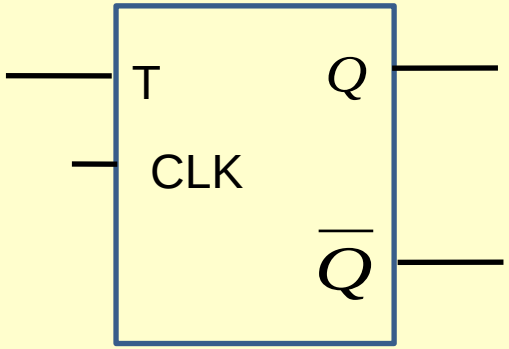
Characteristics table of T FF		
T	Q_{n+1}	
0	Q_n	No Change
1	$\overline{Q_n}$	Toggle

Full State table of T FF		
T	Q_n	Q_{n+1}
0	0	0
0	1	1
1	0	1
1	1	0

$$Q_{n+1}(T, Q_n) = \sum(1,2)$$

T Characteristics equation

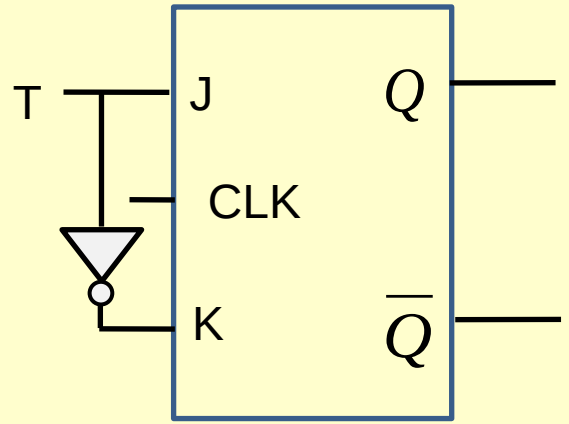
$$Q_{n+1} = T\overline{Q_n} + \overline{T}Q_n = T \oplus Q_n$$



T Flip Flop symbol

D Flip Flop

- D FF is JK FF with J=D and applying NOT gate between J and K
- Output is same as Data input (D)

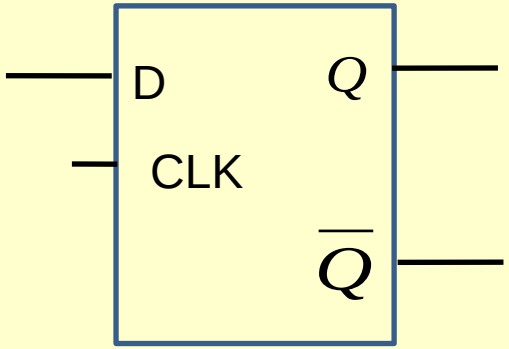


Characteristics table of D FF		
D	Q_{n+1}	
0	0	Reset
1	1	Set

Full State table of T FF		
D	Q_n	Q_{n+1}
0	0	0
0	1	0
1	0	1
1	1	1

$$Q_{n+1}(D, Q_n) = \sum(2,3)$$

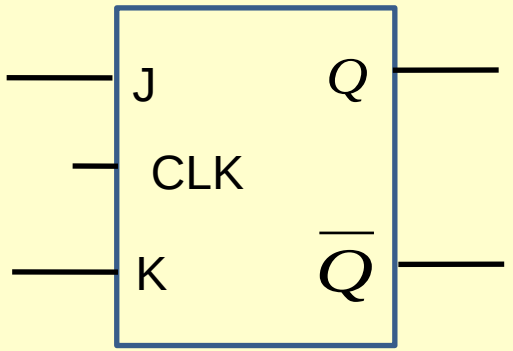
D Characteristics equation $Q_{n+1} = D$



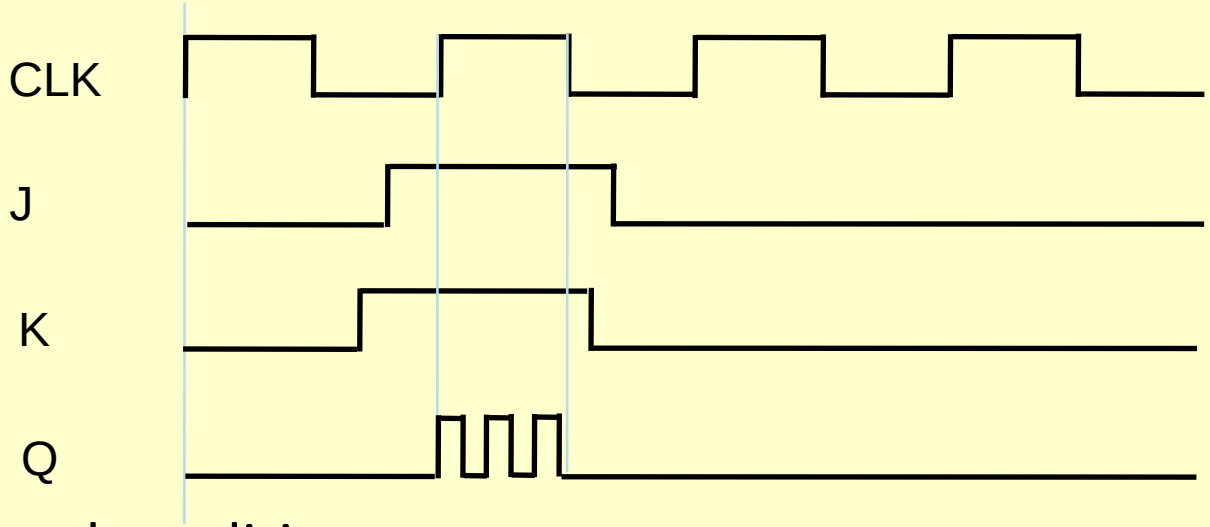
D Flip Flop symbol

JK Flip Flop: Race around condition

- when J=K=1, output toggles recursively during active period of clock pulse
- This leads to unpredictable output state after active period of clock pulse
- This condition is know as race around condition



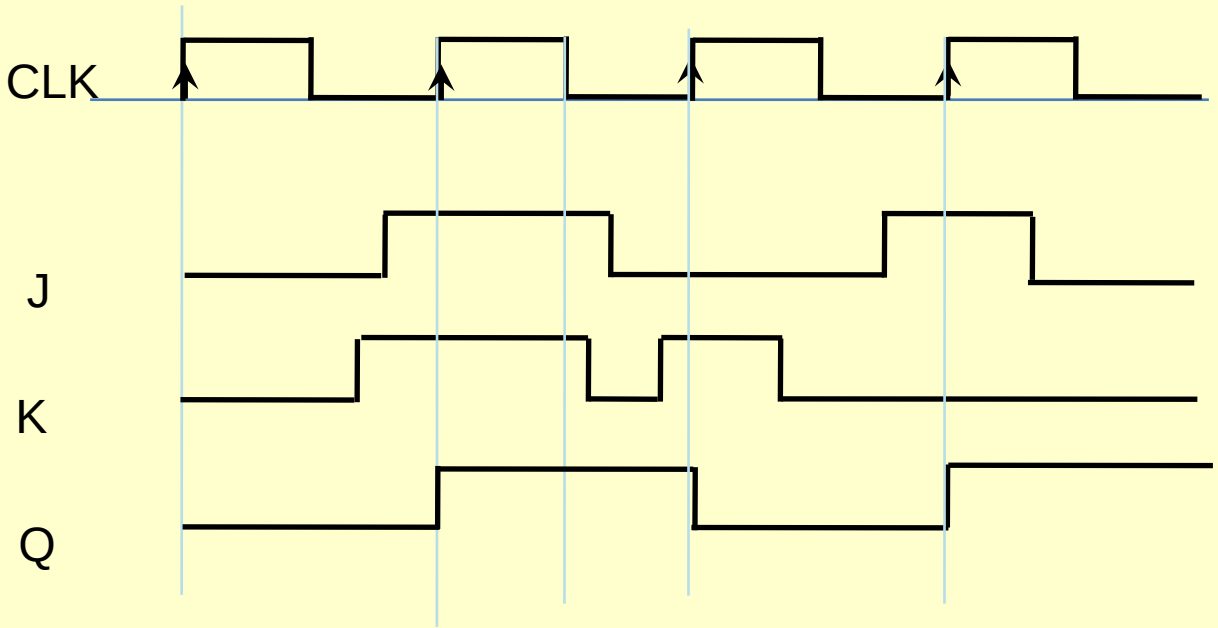
JK Flip Flop symbol



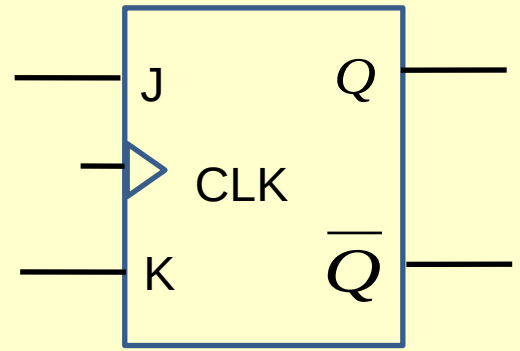
- Solution to race around condition
  - Master slave FF: that gives a single trigger at slave output. How ever race around condition occurs in Master.
  - Edge triggered FF: flip-flop triggers the 'edge' of clock pulse

Edge Triggered Flip Flop

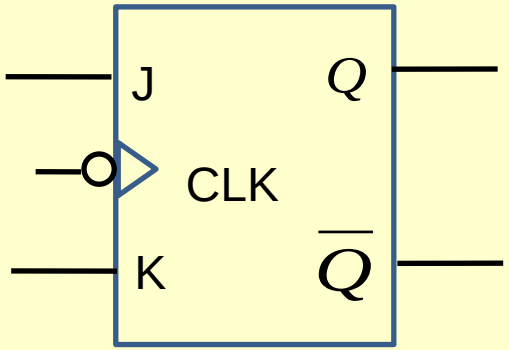
•Edge triggered FF considers input values at the edge of the clock pulse (either positive or negative)



•Timing diagram of typical positive edge triggered JK FF



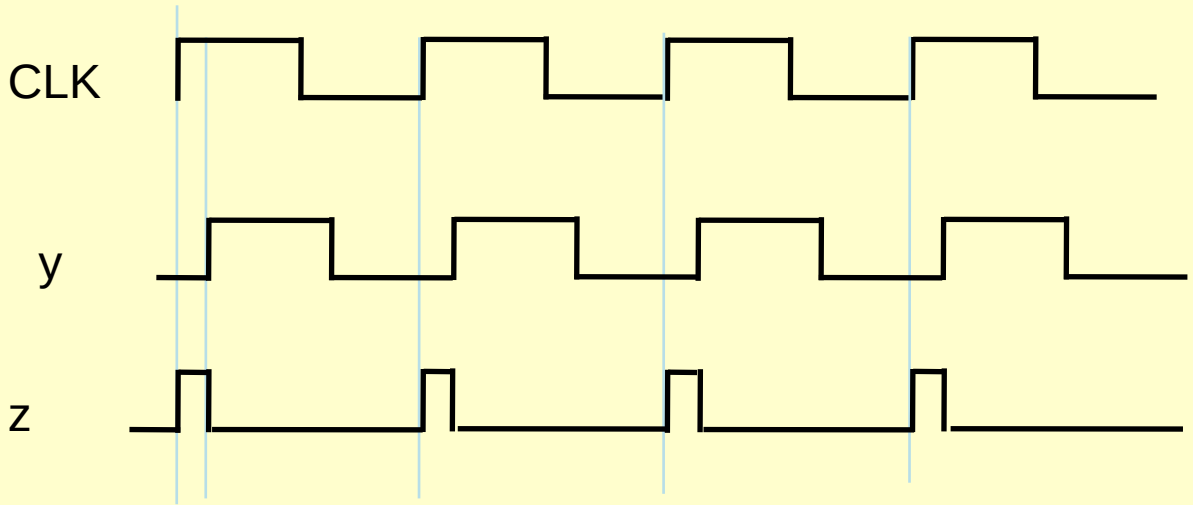
Positive Edge triggered JK FF

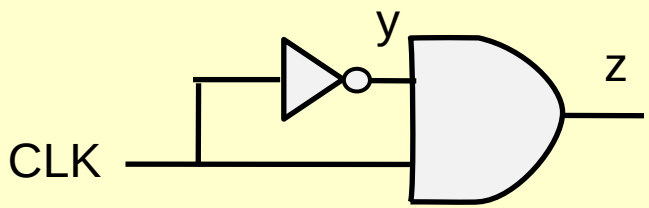


Negative Edge triggered JK FF

Edge Trigger Circuit

•Edge triggered FF considers input values at the edge of the clock pulse (either positive or negative)





Positive edge pulse train generation circuit

•Circuit generates a pulse train of pulse duration equal to delay time of invert gate (comparable to rise time or edge duration of clock pulse)

• Narrow pulse duration allows only one input trigger in clock pulse

Conversion of Flip-flops

T→JK FF conversion

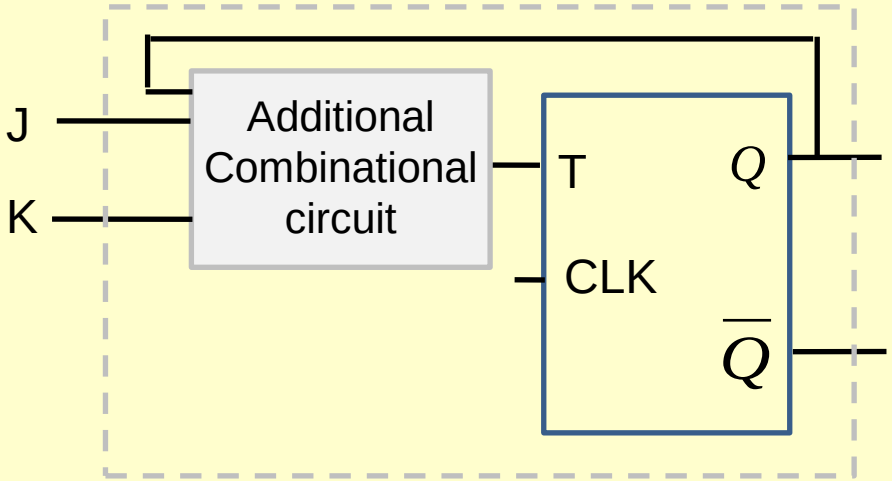
- Requires design of additional combination circuit (as shown in figure)

Step 1: Write the desired state table (JK State table)

Step 2: Determine what should be value at available FF input for desired state changes (what should be at T to cause $Q_n \rightarrow Q_{n+1}$ using excitation table of T

Step 3: Write output of additional circuit (T) in SOP and minimize using K map

Step 4: Implement the function



T FF to JK FF Conversion

Conversion of Flip-flops

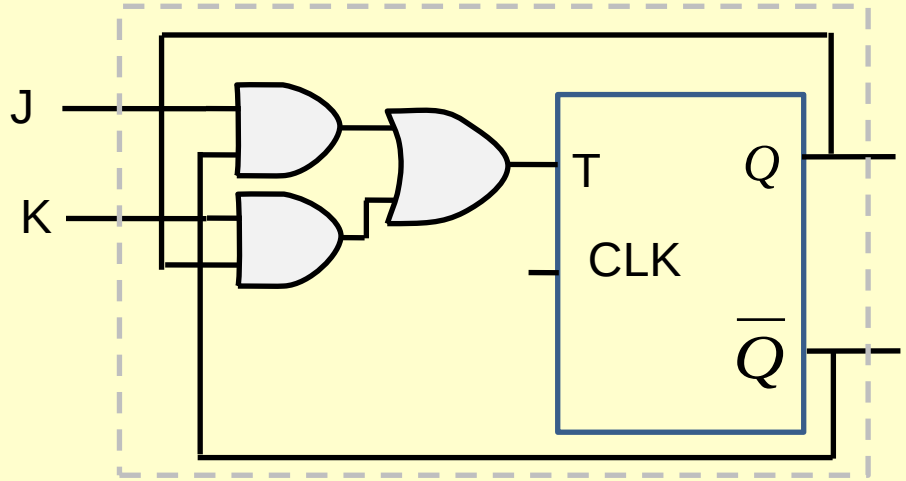
T→JK FF conversion

J	K	Q_n	Q_{n+1}	T
0	0	0	0	0
0	0	1	1	0
0	1	0	0	0
0	1	1	0	1
1	0	0	1	1
1	0	1	1	0
1	1	0	1	1
1	1	1	0	1

$$T(J,K,Q_n) = \sum(3,4,6,7)$$

Solving using K map

$$T = J\overline{Q_n} + KQ$$



T FF to JK FF Conversion

T FF excitation table

Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0